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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,947	10/30/2000	Edmund J. Kelly	TRANS04D	8830
45590 7590 10/17/2008 TRANSMETA C/O MURABITO, HAO & BARNES LLP TWO NORTH MARKET STREET THIRD FLOOR SAN JOSE, CA 95113				
EXAMINER				
THAI, TUAN V				
ART UNIT		PAPER NUMBER		
2185				
MAIL DATE		DELIVERY MODE		
10/17/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/699,947

Applicant(s)

KELLY ET AL.

Examiner

Tuan V. Thai

Art Unit

2186

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08/05/2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5, 18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) 4, 6-17 and 19 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 18 and 20 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Page No(s)/Mail Date 08/05/2008

Part III DETAILED ACTION

Specification

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 05, 2008 has been entered.
2. Claims 1-3, 5, 18 and 20 are presented for examination. Claims 4, 6-17 and 19 have been cancelled.
3. The Information Disclosure Statements filed August 05, 2008 have been reviewed and considered by the Examiner.
4. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.
5. Claims 2 and 5 are objected to under 37 CFR 1.75(c) as being redundant and not further limit independent claim 1.

Applicants are required to 1) cancel the objected claims, or (2) to amend the claims so that they further limit the claim in which they are depended upon.

Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugimoto Koichi (Jap. App. No. 02-054058); hereinafter Koichi, in view of Moore et al. (USPN: 5,437,017); hereinafter Moore.

As per claims 1, 3 and 5; Kochi discloses the invention as claimed including a system for maintaining translation consistency in a computer which includes a host processor (abstract) designed to execute instructions of a host

instruction set and software (embedded in the system of Koichi) for translating instructions from a target instruction set to instructions of the host instruction set (abstract) comprises a hardware means comprises a look-aside buffer (TLB) 3 with an instruction converting unit 2 (e.g. see attached figure) for translating a first address storing a target instruction to a second memory address for use by the host having plurality of storage locations for virtual addresses and associated physical addresses and storage position in each storage location of the TLB (e.g. see attached figure); the software means is known to be embedded in the system of Koichi, particularly considered to be within the instruction converting unit 3, for carrying-out the translating/converting process. Koichi with only one exception does not particularly teaches the software means for removing the at least one host instruction from the second memory address (claims 1 and 5), or invalidating the at least one host instruction at the second memory address (claim 3) for maintaining data consistency within the system. Moore, in his teaching of method and system for maintaining TLB coherency in a multiprocessor data processing system, discloses in maintaining data coherency between all translation look-aside-buffers, (a) the software synchronization is implemented throughout the multiprocessor data processing system; particularly, issuing the

translation lookaside buffer invalidate (TLBI) instruction at all processors within the system (claim 3) (e.g. see column 2, lines 36-37; column 3, lines 12-27; figure 5, column 8, lines 32 et seq.), wherein the removing of the at least one host instruction at the second address is being equivalently taught as terminating the execution of all pending instructions (including host instruction) until after the TLBI instruction has been executed, or suspending execution of all pending instructions until all read and write operations within the memory queue have achieved coherency (claims 1 and 5) (e.g. see column 3, lines 19-27). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the software synchronization and invalidation of data/instruction in a multiprocessing environment as taught by Moore for that of Koichi's system in order to arrive at Applicant's current invention. By removing and invalidating the host instruction from the second memory address, particularly when there is an update or modification of data/instruction within the system, it would prevent other processors or I/O units from executing stale or out-of-date instruction/data; thereby data coherency can be uniformly maintained, therefore being greatly advantageous.

As per claim 2, Koichi discloses translation look-aside buffer (TLB) 3 with an instruction converting unit 2 (e.g. see Koichi's attached figure) for translating a first address storing a target instruction to a second memory address for use by the host having plurality of storage locations for virtual addresses and associated physical addresses and storage position in each storage location of the TLB (e.g. see Abstract's constitution);

Allowable subject matter

8. Claim 18 is allowed. Claim 19 is also allowable since it is depended on the indicated allowable claim 18.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-

272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/October 10, 2008

/Tuan V. Thai/

Primary Examiner, Art Unit 2186